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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/920,042	08/01/2001	Abraham Karel Riemens	NL 010506	5443

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EXAMINER	
QUILLEN, ALLEN E	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 11/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/920,042	RIEMENS ET AL.	
	Examiner	Art Unit	
	Allen E. Quillen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 25 September 2003 .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Claims 1-8 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 2-3, 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Taraci, et al, U.S. Patent 6,316,974.

4. Regarding claim 1, Taraci discloses a processor for executing image processing under control of a clock facility (Column 15, lines 1-14), such that a sequence of **C** effective clock cycles (*vertical sync period*, Column 14, lines 41-44) will effect a processing operation of a

predetermined amount of image information (*required total number of pixels per line of output,* lines 8-10), said processor being characterized in having a programming means (Column 8, lines 35-45) for implementing programmable stall clock cycles (*frame rate delay,* Column 8, lines 46-50) interspersed between said effective clock cycles for implementing a programmable slowdown factor **S** (*scaled,* Column 10, lines 41-43), such that a modified number of **C*S** overall clock cycle will effect processing of said predetermined amount of image information (Column 9, lines 8-45).

5. Regarding claim 2, Taraci discloses a processor as claimed in Claim 1, and having said programming means controlling the interspersing in an at least substantially periodical manner (*for every cycle..computed,* Column 16, lines 19-20).

6. Regarding claim 3, Taraci discloses a processor in Claim 1, effectively representing a coprocessor and having a control processor as said programming means (Figure 8, element 808, Column 14, lines 19-39).

7. Regarding claim 6, Taraci discloses a processor as claimed in Claim 1, and being arranged to execute at least two different image processing operations under (respective, see above) different percentages of stall clock cycles (Column 2, lines 18-65; Column 6, lines 39-43).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 4, 5, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taraci, et al, U.S. Patent 6,316,974, as applied to claims 1 and 3 above, in view of Crump, et al, U.S. Patent 5,638,531.

10. Regarding claim 4, Taraci discloses a processor as claimed in Claim 3, wherein said coprocessor and said control processor are interconnected to a shared memory facility (Column 5, lines 21-36). Taraci does not disclose interconnected by a bus. Crump teaches interconnected by a bus (Column 4, lines 40 through Column 6, line 7). The motivation for combining video image processing using programmable time skew (stall clock cycles) with processors connected by a bus is to enable supporting a wide variety of video display formats involving complicated refresh logic (Column 1, lines 29-45, 58-67). Crump is evidence that at the time of the invention it would have been obvious to one skilled in the art of video image processing to combine the benefits of programmable time skew (stall clock cycles) using multiple processors, as Taraci discloses, with a bus system, as Crump teaches, to enable supporting a wide variety of video display formats.

11. Regarding claim 5, Taraci discloses a processor as claimed in Claim 4, wherein said coprocessor, said control processor and said bus have shared memory facility (see above). Taraci does not disclose are disposed on a single semiconductor chip, whereas said shared memory facility is at least substantially off-chip. Crump teaches are disposed on a single semiconductor chip, whereas said shared memory facility is at least substantially off-chip (Column 2, lines 48-50; Figure 1, element 11, Column 3, lines 4-6, 45-64; Column 4, lines 8-17, 24-26, 53-55). The motivation for combining video image processing using programmable time skew (stall clock cycles) with a chip with processors connected by a bus and a memory is to enable supporting a wide variety of video display formats involving complicated refresh logic

(Column 1, lines 29-45, 58-67). Crump is evidence that at the time of the invention it would have been obvious to one skilled in the art of video image processing to combine the benefits of programmable time skew (stall clock cycles) using multiple processors, as Taraci discloses, with a chip and a bus system with external memory, as Crump teaches, to enable supporting a wide variety of video display formats.

12. Regarding claim 8, Taraci discloses a processor as claimed in Claim 5, Taraci discloses the coprocessor is arranged in an interval during a said stall cycle (see above). Taraci does not disclose wherein at least one other bus station that the coprocessor is arranged and allowed to temporarily grab the bus in an interval during a said stall cycle. Crump teaches wherein at least one other bus station that the coprocessor is arranged and allowed to temporarily grab the bus in an interval during a said stall cycle (Column 4, lines 1-7; Column 6, lines 25-57, *fairness algorithm*). The motivation for combining video image processing using programmable time skew (stall clock cycles) with a chip with processors connected with bus sharing and a memory is to enable supporting a wide variety of video display formats involving complicated refresh logic (Column 1, lines 29-45, 58-67). Crump is evidence that at the time of the invention it would have been obvious to one skilled in the art of video image processing to combine the benefits of programmable time skew (stall clock cycles) using multiple processors, as Taraci discloses, with a chip and bus sharing system with external memory, as Crump teaches, to enable supporting a wide variety of video display formats.

Claim Rejections - 35 USC § 103

13. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Taraci, et al, U.S. Patent 6,316,974, as applied to claims 1 above, in view of Kondoh, et al, U.S. Patent 5,649,119.

14. Regarding claim 7, as best understood by the Examiner, Taraci discloses a processor as claimed in claim 1, wherein said programming means drive an incremental storage facility through a periodical increment by a number **N** that is a function of said factor S according to **N = round (R*x),** wherein **x= (S-1/S)** and **R** is the range of the storage facility (slowdown factor S >= 1, per page 5, lines 16-18. Where **S**=1, **x**=0, then **N**=0, see example at Column 14, lines 40-67). Taraci does not disclose wherein a carry output signal of the storage facility will generate an effective clock cycle. Kondoh teaches a carry output signal of the storage facility will generate an effective clock cycle (Column 1, lines 10-12; Column 19, lines 15-38). The motivation for combining video image processing using programmable time skew (stall clock cycles) using cycle range and slowdown factor algorithm with storage facility carry output signal to generate an effective clock cycle is to enable efficient data queuing particularly with packet addressing (Column 1, lines 10-12, 25-30; Column 2, lines 50-67). Kondoh is evidence that at the time of the invention it would have been obvious to one skilled in the art of video multimedia image processing to combine the benefits of programmable time skew algorithm, as Taraci discloses, with cycle range and slowdown factor algorithm with storage facility carry output signal to generate an effective clock cycle, as Kondoh teaches, to enable efficient packet-based addressing to prevent loss of information particularly when reading low priority data (Column 19, line 32-33).

Response to Arguments

15. Applicant asserts that "reference [Taraci] reference lacks at least a disclosure of the use of a programmable stall clock cycles to slow down processing." (page 7, paragraph 3); and "image processing is not really addressed..." (page 7, paragraph 4).

16. The Examiner respectfully replies, however, that, *in the claims*, Taraci discloses said processor being characterized in having a programming means (Column 8, lines 35-45) for implementing programmable stall clock cycles (*frame rate delay*, Column 8, lines 46-50; Figure 11, *shift clock, load_clock;* Figure 12, *PIX_CLK, ~64MHZ*) interspersed between said effective clock cycles for implementing a programmable slowdown factor **S** (*scaled,* Column 10, lines 41-43), such that a modified number of **C*S** overall clock cycle will effect processing of said predetermined amount of image information (*Graphics environment, pixels, video frame rates, display, digital video, camera panning, solve the graphics switcher new input "jitter" problem, These input video signals are scaled to match the output video requirement and are subsequently output at high rates to a display device.* Column 10, lines 40-43; Abstract, Column 5, lines 65-67; Column 1, lines 20-28, Column 9, lines 8-45).

Conclusion

17. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen E. Quillen whose telephone number is (703) 605-4584. The examiner can normally be reached on Tuesday – Friday, 8:30am – noon and 1:00 - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Bella, can be reached on (703) 308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or FAX'd to: (703) 872-9314 (for Technology Center 2600 only)

Hand delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Sixth Floor (Receptionist), Arlington, Virginia

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number (703) 305-9600 or (703) 305-3800.

Allen E. Quillen
Patent Examiner
Art Unit 2676

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November 19, 2003

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600